What is claimed is:

1. A DLL (delay locked loop) circuit comprising:

a delay circuit which is connected to first and second nodes, and which delays an original clock signal supplied to said first node based on a delay control signal and generates first to n-th (n is an integer more than 1) internal clock signals, wherein said first internal clock signal is outputted from said second node, and the internal clock signals other than said first internal clock signal are outputted from said delay circuit without passing through said second node, and lead the first internal clock signal in phase;

a phase comparing circuit which compares said original clock signal supplied from said first node and said first internal clock signal supplied from said second node, and outputs a phase difference of said original clock signal and said first internal clock signal; and

a delay control circuit which outputs said delay control signal to said delay circuit based on the phase difference outputted from said phase comparing circuit.

2. The DLL circuit according to claim 1, wherein said delay circuit comprises:

a first delay section which delays said

original clock signal based on said delay control signal to generate a first delay signal; and

a second delay section which is provided between said second node and said first delay section, and delays the first delay signal to generate said first to n-th internal clock signals, and outputs said first internal clock signal from said second node, and the internal clock signals other than said first internal clock signal without passing through said second node.

3. The DLL circuit according to claim 2, wherein said second delay circuit comprises:

a plurality of delay elements connected in series, and said first to n-th internal clock signals are outputted from different ones of said plurality of delay elements.

4. The DLL circuit according to claim 3, wherein said plurality of delay elements have substantively a same delay quantity.

5. The DLL circuit according to claim 3, wherein said plurality of delay elements have delay quantities different from each other.

6. The DLL circuit according to claim 3, wherein

a delay quantity of each of said plurality of delay elements is predetermined.

7. The DLL circuit according to claim 3, wherein a delay quantity of each of said plurality of delay elements is independent of a frequency of said original clock signal.

8. The DLL circuit according to claim 3, wherein each of said plurality of delay elements is one of an inverter and a buffer.

9. The DLL circuit according to claim 3, wherein the number of delay elements is n.

10. A semiconductor memory device, comprising:

a DLL (delay locked loop) circuit which is connected to a node and delays an external clock signal to generate first and second internal clock signals, said first internal clock signal is outputted through said node, said second internal clock signal leads said first internal clock signal by a predetermined phase value;

a first flip-flop which generates a latch signal in response to said first internal clock signal;

a second flip-flop which generates a read

enable signal in response to said second internal clock signal; and

a memory section which includes a memory cell array, and prepares a read operation of data from said memory cell array in response to the read enable signal and latches the data in response to the latch signal.

11. The semiconductor memory device according to claim 10, wherein said predetermined phase value corresponds to a time of precharging read lines associated with the read operation of the data.

12. The semiconductor memory device according to claim 10, wherein said DLL circuit comprises:

a delay circuit which is connected to said node, and which delays said external clock signal based on a delay control signal and generates said first and second internal clock signals, wherein said second internal clock signal is outputted without passing through said node;

a phase comparing circuit which compares said external clock signal supplied and said first internal clock signal, and outputs a phase difference of said external clock signal and said first internal clock signal; and

a delay control circuit which outputs said

delay control signal to said delay circuit based on the phase difference outputted from said phase comparing circuit.

13. The semiconductor memory device according to claim 12, wherein said delay circuit comprises:

a first delay section which delays said external clock signal based on said delay control signal to generate a first delay signal; and

a second delay section which is connected to said node and delays the first delay signal to generate said first and second internal clock signals.

14. The semiconductor memory device according to claim 13, wherein said second delay circuit comprises:

a plurality of delay elements connected in series, and said first and second internal clock signals are outputted from different ones of said plurality of delay elements, respectively.

15. The semiconductor memory device according to claim 14, wherein a delay quantity of each of said plurality of delay elements is independent of a frequency of said external clock signal.

16. The semiconductor memory device according to claim 14, wherein a delay quantity of each of said

plurality of delay elements is predetermined.

17. A method of generating timing signals comprising the steps of:

(a) delaying an original clock signal supplied to a first node based on a delay control signal;

(b) generating first to n-th (n is an integer more than 1) internal clock signals from the delayed original clock signal, wherein said first internal clock signal is outputted from a second node, and the internal clock signals other than said first internal clock signal are outputted without passing through the second node, and lead said first internal clock signal in phase by a predetermined value;

(c) detecting a phase difference between said original clock signal and said first internal clock signal; and

(d) generating said delay control signal based on the detected phase difference.

18. The method according to claim 17, wherein the (a) delaying step comprises the steps of:

(e) delaying said original clock signal based on said delay control signal to generate a first delay signal; and

(f) delaying the first delay signal to

generate said first to n-th internal clock signals.

19. The method according to claim 18, wherein the (f) delaying step comprises the step of:

(g) delaying the first delay signal by a plurality of delay elements connected in series, wherein said first to n-th internal clock signals are outputted from different ones of said plurality of delay elements.

20. The method according to claim 19, wherein said plurality of delay elements have substantively a same delay quantity.

21. The method according to claim 19, wherein said plurality of delay elements have delay quantities different from each other.

22. The method according to claim 19, wherein a delay quantity of each of said plurality of delay elements is predetermined.

23. The method according to claim 19, wherein a delay quantity of each of said plurality of delay elements is independent of a frequency of said original clock signal.